**WHAT IS CLAIMED IS:**

1. A method of improving reliability of an underfilled semiconductor device comprising at least one layer of low-K ILD, steps of which comprise:

providing a semiconductor device comprising:

a semiconductor chip comprising copper electrical interconnections and at least one layer of low-K ILD therewithin and metallization on a surface thereof; and

a carrier substrate having electrical contact pads on a surface thereof to which the semiconductor chip is electrically interconnected through an electrically conductive material to the copper electrical interconnections;

providing a heat curable underfill composition between the electrically interconnected surfaces of the semiconductor chip and the carrier substrate to form a semiconductor device assembly; and

exposing the semiconductor device assembly to elevated temperature conditions sufficient to cure the heat curable underfill composition,

wherein the heat curable underfill composition comprises a curable resin component and a filler component, wherein the filler component is present in an amount sufficient to provide the heat curable underfill composition when cured with a coefficient of thermal expansion of less than about 25 ppm/°C or a coefficient of thermal expansion of greater than about 50 ppm/°C and when cured the heat curable underfill composition has a ratio of modulus versus temperature between -65°C and 125°C in the range of 10MPa/°C to about -10MPa/°C.

2. The method of Claim 1, wherein after the semiconductor chip and the carrier substrate are mated the

heat curable underfill composition is provided by dispensing and filling the space therebetween to form the semiconductor device.

3. The method of Claim 1, wherein the heat curable underfill composition is provided by dispensing onto at least a portion of an electrically interconnecting surface of one or both of the semiconductor chip or the carrier substrate, and the semiconductor chip and the carrier substrate are then mated to form the semiconductor device.

4. The method of Claim 1, wherein the carrier substrate is a circuit board.

5. The method of Claim 1, wherein the electrically conductive material is solder.

6. The method of Claim 5, wherein the solder is selected from the group consisting of Sn(63):Pb(37), Pb(95):Sn(5), Sn:Ag(3.5):Cu(0.5) and Sn:Ag(3.3):Cu(0.7).

7. A semiconductor device comprising:

a semiconductor chip comprising copper electrical interconnections and the layer of low-K ILD therewithin and metallization on a surface thereof;

a circuit board having electrical contact pads on a surface thereof to which the semiconductor chip is electrically interconnected; and

a heat curable underfill composition between the semiconductor chip and the circuit board,

wherein the heat curable underfill composition comprises a curable resin component and a filler component, wherein the filler component is present in an amount sufficient to provide the heat curable underfill composition when cured with a coefficient of thermal expansion of less than about 25 ppm/°C or a coefficient of thermal expansion of greater

than about 50 ppm/°C, and wherein the heat curable underfill composition has a ratio of modulus versus temperature between -65°C and 125°C in the range of -10MPa/°C to about 10MPa/°C.

8. The method of Claim 7, wherein the electrically conductive material is solder.

9. The method of Claim 8, wherein the solder is selected from the group consisting of Sn(63):Pb(37), Pb(95):Sn(5), Sn:Ag(3.5):Cu(0.5) and Sn:Ag(3.3):Cu(0.7).

10. A semiconductor device assembly comprising:

a semiconductor device comprising a semiconductor chip comprising copper electrical interconnections thereof contacting at least one layer of low-K ILD therewithin, therewithin and metallization on a surface thereof to which is electrically connected a carrier substrate;

a circuit board having electrical contact pads on a surface thereof to which the semiconductor device is electrically interconnected; and

a heat curable underfill composition between the semiconductor device and the circuit board,

wherein the heat curable underfill composition comprises a curable resin component and a filler component, wherein the filler component is present in an amount sufficient to provide the heat curable underfill composition when cured with a coefficient of thermal expansion of less than about 25 ppm/°C or a coefficient of thermal expansion of greater than about 50 ppm/°C, and wherein the heat curable underfill composition has a ratio of modulus versus temperature between -65°C and 125°C in the range of -10MPa/°C to about 10MPa/°C.

11. The method of Claim 10, wherein the electrically conductive material is solder.

12. The method of Claim 11, wherein the solder is selected from the group consisting of Sn(63):Pb(37), Pb(95):Sn(5), Sn:Ag(3.5):Cu(0.5) and Sn:Ag(3.3):Cu(0.7)

13. An integrated circuit chip comprising a semiconductor chip having electrical contacts arranged in a predetermined pattern and capable of providing electrical engagement with a carrier substrate, the circuit chip comprising:

a fluxing agent contacting the electrical contacts; and

a heat curable underfill composition distinct from the fluxing agent and in contact with the chip die; and

optionally, a thermosetting composition, reaction products of which are controllably degradable when exposed to appropriate conditions,

wherein, when present, the thermosetting composition is distinct from the fluxing agent and the heat curable underfill composition and is in contact with the heat curable underfill composition;

wherein the electrical contacts are flowable to provide the electrical engagement with the carrier substrate, the heat curable underfill composition and, when present, the thermosetting composition are curable for adhering the circuit chip to the carrier substrate, and, when present, the thermosetting composition being controllably degradable to release the circuit chip from the carrier substrate, wherein the heat curable underfill composition comprises a curable resin component and a filler component, wherein the filler component is present in an amount sufficient to provide the heat curable underfill composition when cured with a coefficient of thermal expansion of less than about

25 ppm/°C or a coefficient of thermal expansion of greater than about 50 ppm/°C, and wherein when cured the heat curable underfill composition has a ratio of modulus versus temperature between -65°C and 125°C in the range of -10MPa/°C to about 10MPa/°C.

14. The method of Claim 13, wherein the electrically conductive material is solder.

15. The method of Claim 14, wherein the solder is selected from the group consisting of Sn(63):Pb(37), Pb(95):Sn(5), Sn:Ag(3.5):Cu(0.5) and Sn:Ag(3.3):Cu(0.7).

16. An integrated circuit chip assembly comprising:

a circuit board; and

a semiconductor chip adhered to the circuit board through a heat curable underfill component and optionally, a thermosetting component, reaction products of the thermosetting component being controllably degradable when exposed to appropriate conditions, the thermosetting component capable of controllable degradation to release the chip die from the circuit board substrate, the chip die including electrical contacts in electrical engagement with the circuit board substrate, the electrical engagement achieved through bonding of the electrical contacts to the circuit board substrate through a fluxing agent, the fluxing agent being distinct from the heat curable underfill component and the thermosetting component, and wherein the heat curable underfill composition comprises a curable resin component and a filler component, wherein the filler component is present in an amount sufficient to provide the heat curable underfill composition when cured with a coefficient of thermal expansion of less than about 25 ppm/°C or a coefficient of thermal expansion of greater

than about 50 ppm/°C, and wherein when cured the heat curable underfill composition has a ratio of modulus versus temperature between -65°C and 125°C in the range of -10MPa/°C to about 10MPa/°C.

17. The method of Claim 16, wherein the electrically conductive material is solder.

18. The method of Claim 17, wherein the solder is selected from the group consisting of Sn(63):Pb(37), Pb(95):Sn(5), Sn:Ag(3.5):Cu(0.5) and Sn:Ag(3.3):Cu(0.7).

19. A method for assembling an integrated circuit assembly, steps of which comprise:

providing an integrated circuit chip in accordance with Claim 13;

joining the integrated circuit chip with a carrier substrate to form a mated assembly; and

exposing the assembly formed in step (b) to elevated temperature conditions sufficient to render the electrical contacts flowable and cure the heat curable underfill composition, thereby establishing electrical interconnection in adhering the integrated circuit chip to the carrier substrate.

20. A method for assembling an integrated circuit chip, steps of which comprise:

providing a semiconductor chip having electrical contacts arranged in a predetermined pattern thereon;

applying a fluxing agent over at least a portion of the electrical contacts; and

dispensing a heat curable underfill composition in a flowable form on the semiconductor chip around the electrical contacts, the heat curable underfill composition being distinct from the fluxing agent, and wherein the heat curable underfill composition comprises a curable resin

component and a filler component, wherein the filler component is present in an amount sufficient to provide the heat curable underfill composition when cured with a coefficient of thermal expansion of less than about 25 ppm/°C or a coefficient of thermal expansion of greater than about 50 ppm/°C, and wherein when cured the heat curable underfill composition has a ratio of modulus versus temperature between -65°C and 125°C in the range of -10MPa/°C to about 10MPa/°C.

21. The method of Claim 20, wherein the electrically conductive material is solder.

22. The method of Claim 21, wherein the solder is selected from the group consisting of Sn(63):Pb(37), Pb(95):Sn(5), Sn:Ag(3.5):Cu(0.5) and Sn:Ag(3.3):Cu(0.7).

23. A method of assembling a semiconductor device with improved reliability, steps of which comprise:

providing a semiconductor chip having opposed surfaces, one of which for bonding to a carrier substrate and the other of which having electrical interconnections for establishing electrical interconnection therewith, and having a thickness of less than 100 microns;

providing a carrier substrate having a portion of a surface for bonding the semiconductor chip and another portion of a surface for establishing electrical interconnection with the semiconductor chip;

providing a heat curable die attach composition onto at least a portion of one or both of the bonding surface of the semiconductor chip or the bonding surface of the carrier substrate, in an amount sufficient to establish a bondline of less than about 10 microns when the semiconductor chip and the carrier substrate are mated;

mating the bonding surface of the semiconductor chip with the bonding surface of the carrier substrate to form a semiconductor device assembly and exposing the semiconductor device assembly to elevated temperature conditions sufficient to cure the heat curable die attach composition, thereby bonding the semiconductor device to the carrier substrate; and

establishing electrical interconnections between the semiconductor device and the carrier substrate, wherein when cured the heat curable die attach composition has a ratio of modulus versus temperature between -65°C and 125°C in the range of -10MPa/°C to about -10MPa/°C.

24. The method of Claim 23, wherein the heat curable die attach composition comprises a curable resin component and a filler component, wherein the filler component is present in an amount sufficient to provide the heat curable die attach composition when cured with a coefficient of thermal expansion of less than about 25 ppm/°C or a coefficient of thermal expansion of greater than about 50 ppm/°C.

25. A semiconductor device comprising:

a semiconductor chip having opposed surfaces, one of which for bonding to a carrier substrate and the other of which having electrical interconnections for establishing electrical interconnection therewith, and having a thickness of less than 100 microns;

a carrier substrate having a portion of a surface for bonding the semiconductor chip and another portion of a surface for establishing electrical interconnection with the semiconductor chip; and

a die attach composition between the bonding surfaces of the semiconductor chip and the carrier

substrate, to form a bond line of less than about 10 microns,

wherein the die attach composition has a ratio of modulus versus temperature between -65°C and 125°C in the range of -10MPa/°C to about 10MPa/°C.

26. The device of Claim 25, wherein the die attach underfill composition comprises a curable resin component and a filler component, wherein the filler component is present in an amount sufficient to provide the die attach composition when cured with a coefficient of thermal expansion of less than about 25 ppm/°C or a coefficient of thermal expansion of greater than about 50 ppm/°C.

27. The method of Claim 23, wherein the die attach composition comprises a filler.

28. The method of Claim 27, wherein the filler is conductive.

29. The method of Claim 28, wherein the filler is electrically conductive.

30. The method of Claim 28, wherein the filler is thermally conductive.

31. The method of Claim 27, wherein the filler is non-conductive.

32. The method of Claim 27, wherein the filler is teflon.

33. The method of Claim 27, wherein the filler is silica.

34. The semiconductor device of Claim 25, wherein the carrier substrate is a circuit board.

35. A method of improving reliability of a semiconductor device comprising a semiconductor chip

comprising at least one layer of low-K ILD, steps of which comprise:

providing a semiconductor device comprising:

a first semiconductor chip comprising copper electrical interconnections and a layer of low-K ILD therewithin and metallization on a surface thereof; and

a second semiconductor chip having opposed surfaces, one of which for bonding to a carrier substrate and the other of which for establishing electrical interconnection with both the first semiconductor chip and the carrier substrate, wherein the carrier substrate has electrical contact pads on a surface thereof to which at least one of the first semiconductor chip or the second semiconductor chip is electrically interconnected;

providing a first curable composition between the second semiconductor chip and the carrier substrate;

providing a second curable composition between the first semiconductor chip and the second semiconductor chip to form a semiconductor device assembly; and

exposing the semiconductor device assembly to conditions sufficient to cure the first and second compositions, wherein when cured at least one of the compositions has a ratio of modulus versus temperature between -65°C and 125°C in the range of -10MPa/°C to about 10MPa/°C.

36. The method of Claim 35, wherein the first composition comprises a curable resin component and a filler component, wherein the filler component is present in an amount sufficient to provide the first composition when cured with a coefficient of thermal expansion of less than about 25 ppm/°C or greater than about 50 ppm/°C.

37. The method of Claim 35, wherein the second composition comprises a curable resin component and a filler component, wherein the filler component is present in an amount sufficient to provide the second composition when cured with a coefficient of thermal expansion of less than about 25 ppm/°C or greater than about 50 ppm/°C.

38. A semiconductor device comprising:

a first semiconductor chip comprising copper electrical interconnections on a surface thereof over which and at least one layer of low-K ILD therewithin and metallization on a surface thereof;

a second semiconductor chip having opposed surfaces, one of which for bonding to a carrier substrate and the other of which for establishing electrical interconnection with both the first semiconductor chip and the carrier substrate, wherein the carrier substrate has electrical contact pads on a surface thereof to which at least one of the first semiconductor chip or the second semiconductor chip is electrically interconnected; and

a first composition between the second semiconductor chip and carrier substrate;

a second composition between the first semiconductor chip and the second semiconductor chip wherein at least one of the first or the second compositions has a ratio of modulus versus temperature between -65°C and 125°C in the range of -10MPa/°C to about 10MPa/°C.

39. The semiconductor device of Claim 38, wherein the first composition comprises a curable resin component and a filler component, wherein the filler component is present in an amount sufficient to provide the first composition when cured with a coefficient of thermal

expansion of less than about 25 ppm/°C or greater than about 50 ppm/°C.

40. The semiconductor device of Claim 38, wherein the second composition comprises a curable resin component and a filler component, wherein the filler component is present in an amount sufficient to provide the second composition when cured with a coefficient of thermal expansion of less than about 25 ppm/°C or greater than about 50 ppm/°C.

41. A semiconductor device comprising:

a first semiconductor chip comprising copper electrical interconnections on a surface thereof over which and at least one layer of low-K ILD therewithin and metallization on a surface thereof;

a second semiconductor chip having opposed surfaces, one of which for bonding to a carrier substrate and the other of which for establishing electrical interconnection with both the first semiconductor chip and the carrier substrate, wherein the carrier substrate has electrical contact pads on a surface thereof to which at least one of the first semiconductor chip or the second semiconductor chip is electrically interconnected; and

a first composition between the second semiconductor chip and carrier substrate;

a second composition between the first semiconductor chip and the second semiconductor chip to form a semiconductor device assembly,

wherein at least one of the first or the second compositions has a ratio of modulus versus temperature between -65°C and 125°C in the range of -10MPa/°C to about 10MPa/°C.

42. The semiconductor device of Claim 41 wherein the first composition comprises a curable resin component and a filler component, wherein the filler component is present in an amount sufficient to provide the first composition when cured with a coefficient of thermal expansion of less than about 25 ppm/°C or a coefficient of thermal expansion of greater than about 50 ppm/°C.

43. The semiconductor device of Claim 41 wherein the second composition comprises a curable resin component and a filler component, wherein the filler component is present in an amount sufficient to provide the second composition when cured with a coefficient of thermal expansion of less than about 25 ppm/°C or a coefficient of thermal expansion of greater than about 50 ppm/°C.

44. The semiconductor device of Claim 41, wherein the carrier substrate is a circuit board.

45. A method of improving reliability of a semiconductor device comprising at least one layer of low-K ILD, steps of which comprise:

providing a semiconductor device comprising:

a semiconductor chip comprising copper electrical interconnections and at least one layer of low-K ILD therewithin and metallization on a surface thereof; and

a carrier substrate having electrical contact pads on a surface thereof to which the semiconductor chip is electrically interconnected;

providing a heat curable molding compound over the semiconductor device and exposing the semiconductor device to elevated temperature conditions sufficient to cure the heat curable molding compound,

wherein the curable molding compound has a ratio of modulus versus temperature between -65°C and 125°C in the range of -10MPa/°C to about 10MPa/°C.

46. The method of Claim 45, wherein the heat curable molding compound comprises a curable resin component and a filler component, wherein the filler component is present in an amount sufficient to provide the heat curable molding compound when cured with a coefficient of thermal expansion of less than about 25 ppm/°C or a coefficient of thermal expansion of greater than about 50 ppm/°C.

47. An encapsulated semiconductor device comprising:

a semiconductor device comprising:

a semiconductor chip comprising copper electrical interconnections and at least one layer of low-K ILD therewithin and metallization on a surface thereof; and

a carrier substrate having electrical contact pads on a surface thereof to which the semiconductor chip is electrically interconnected; and

a cured molding compound thereover, wherein the molding compound has a ratio of modulus versus temperature between -65°C and 125°C in the range of -10MPa/°C to about 10MPa/°C.

48. The encapsulated semiconductor device of Claim 47, wherein the molding compound comprises a curable resin component and a filler component, wherein the filler component is present in an amount sufficient to provide the cured molding compound with a coefficient of thermal expansion of less than about 25 ppm/°C or a coefficient of thermal expansion of greater than about 50 ppm/°C.

49. The encapsulated semiconductor device of Claim 47, wherein the semiconductor device further comprises a second semiconductor ship electrically interconnected with the semiconductor chip.

50. A heat curable composition comprising:

a curable component selected from the group consisting of an epoxy resin component, a benzoxazine component, and combinations thereof; and

a curative component selected from the group consisting of an anhydride component, a nitrogen-containing compound, a cationic catalyst, and combinations thereof; and wherein a filler component is present in an amount sufficient to provide the heat curable composition when cured with a coefficient of thermal expansion of less than about 25 ppm/°C or a coefficient of thermal expansion of greater than about 50 ppm/°C, and wherein when cured the heat curable composition has a ratio of modulus versus temperature between -65°C and 125°C in the range of -10MPa/°C to about 10MPa/°C.

51. The heat curable composition of Claim 50, suitable for use as an electronic packaging material selected from the group consisting of underfills, die attachment adhesives, liquid encapsulants, molding compounds and end cap encapsulants.